

FIG. 1A

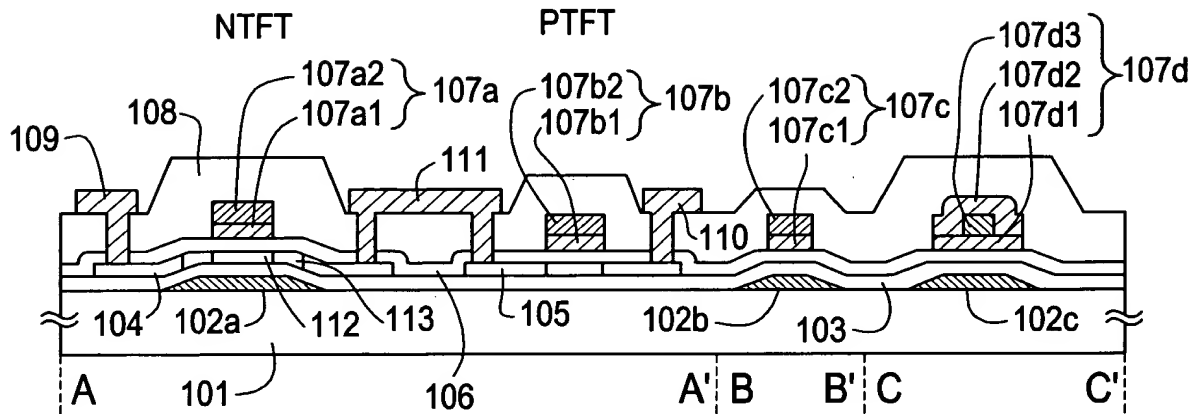


FIG. 1B

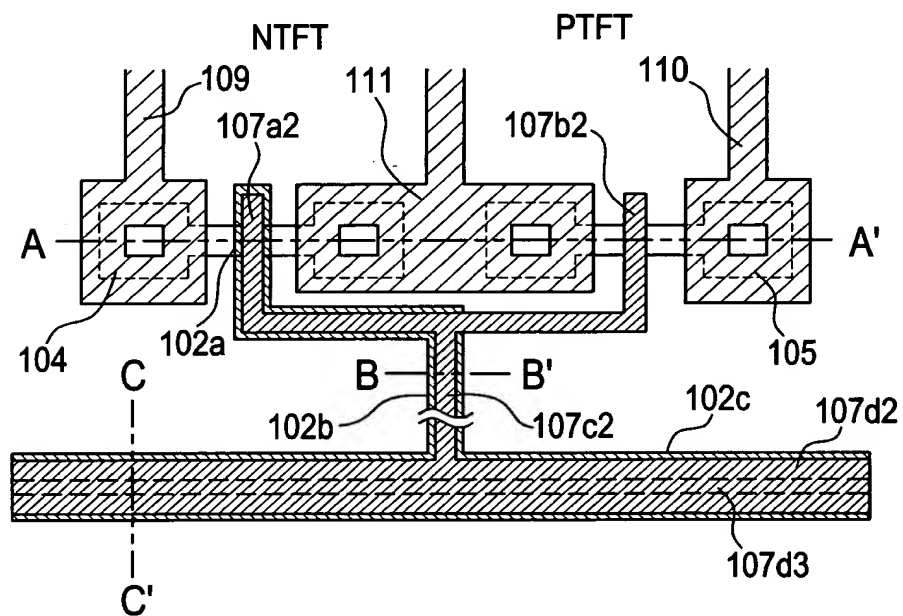


FIG. 2A

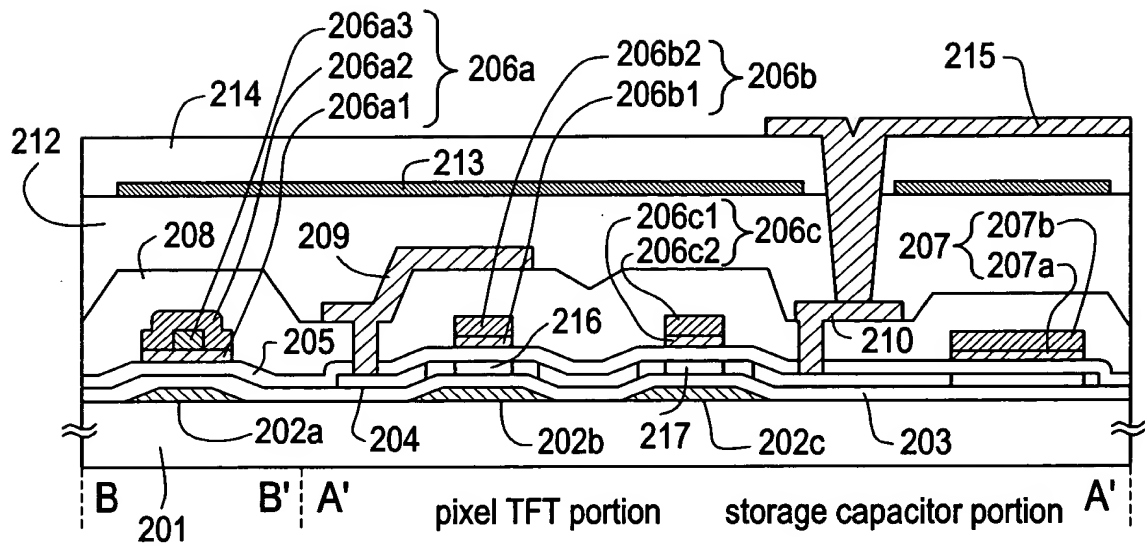


FIG. 2B

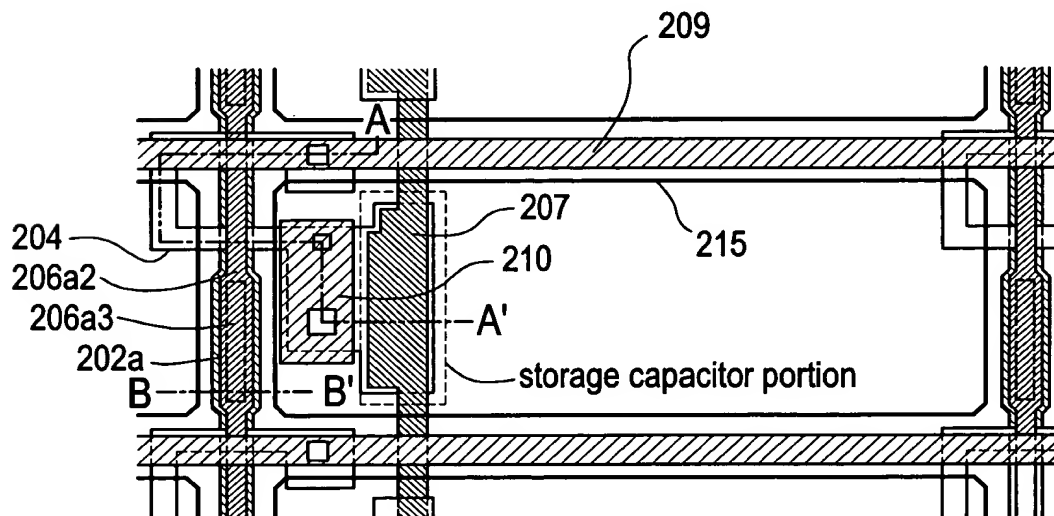


FIG. 3A

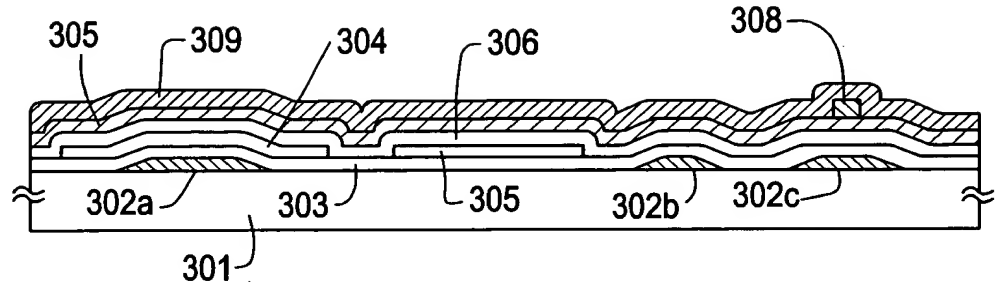


FIG. 3B

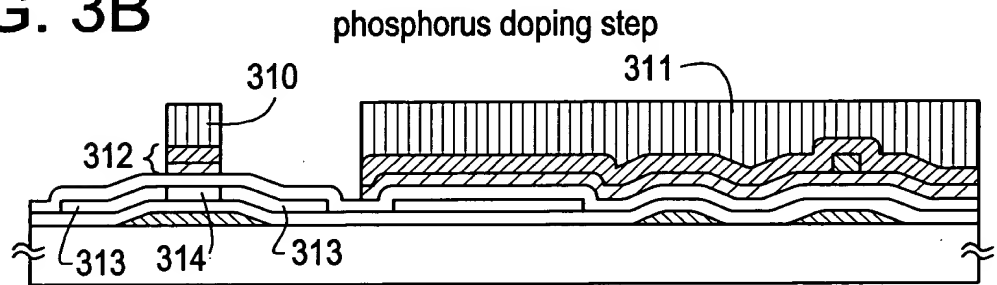


FIG. 3C

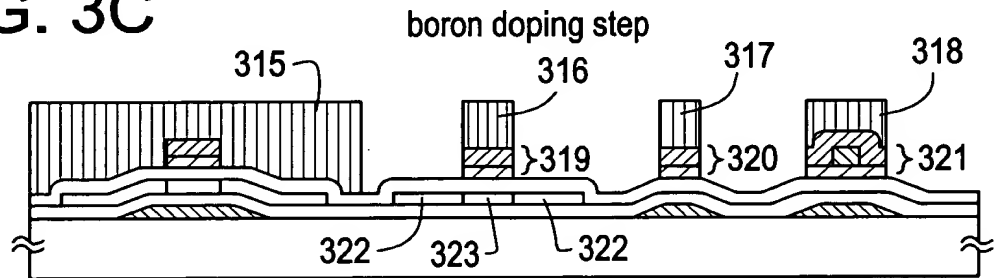


FIG. 3D

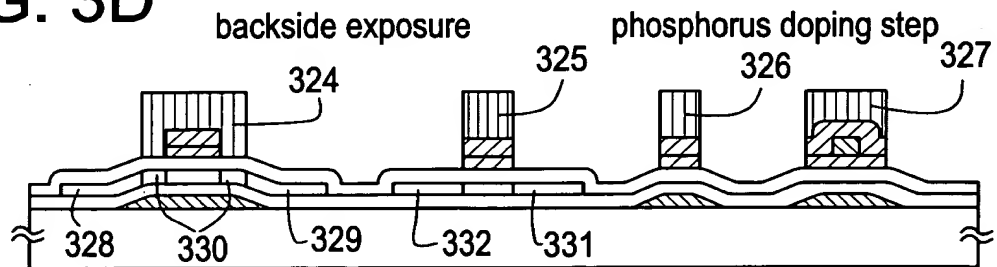


FIG. 3E

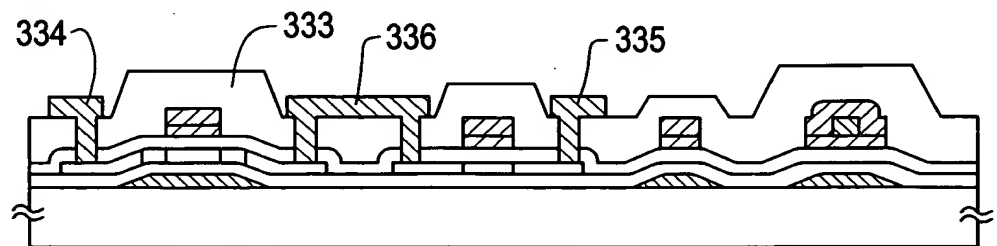


FIG. 4A

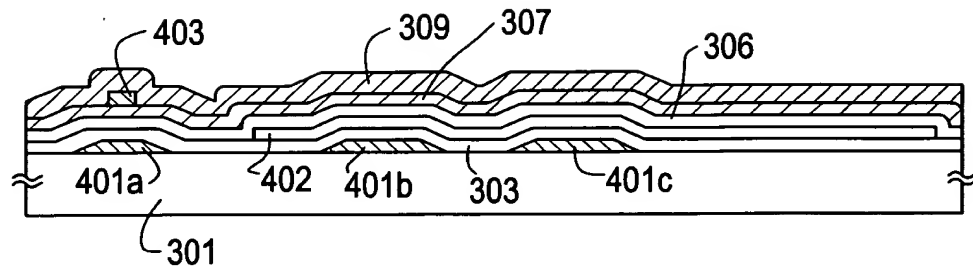


FIG. 4B

phosphorus doping step

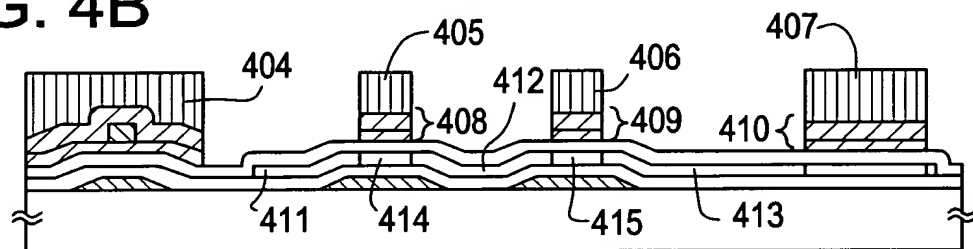


FIG. 4C

boron doping step

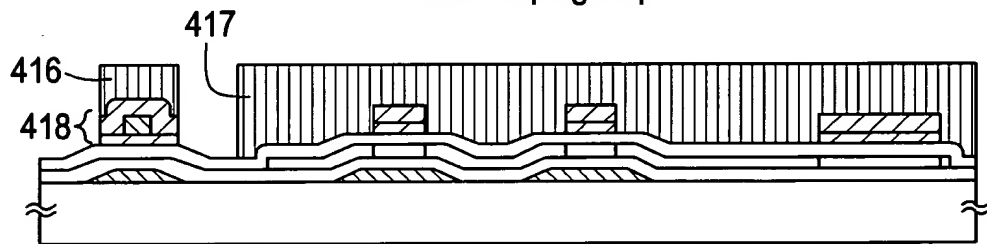


FIG. 4D

backside exposure

phosphorus doping step

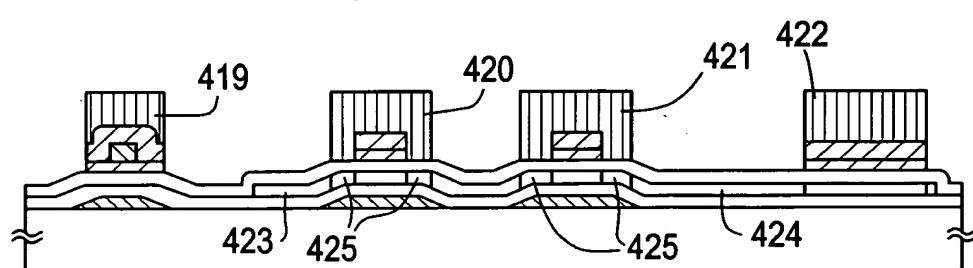


FIG. 4E

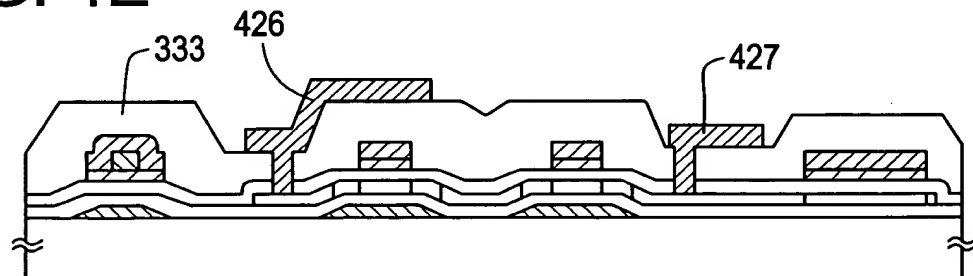


FIG. 5A

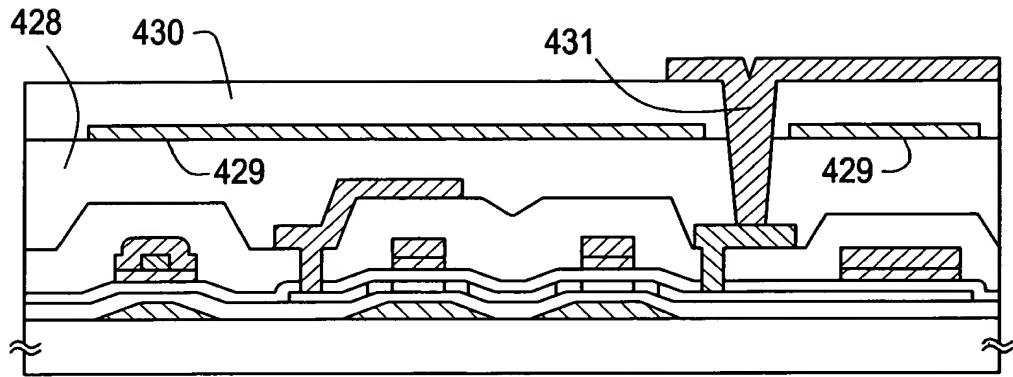


FIG. 5B

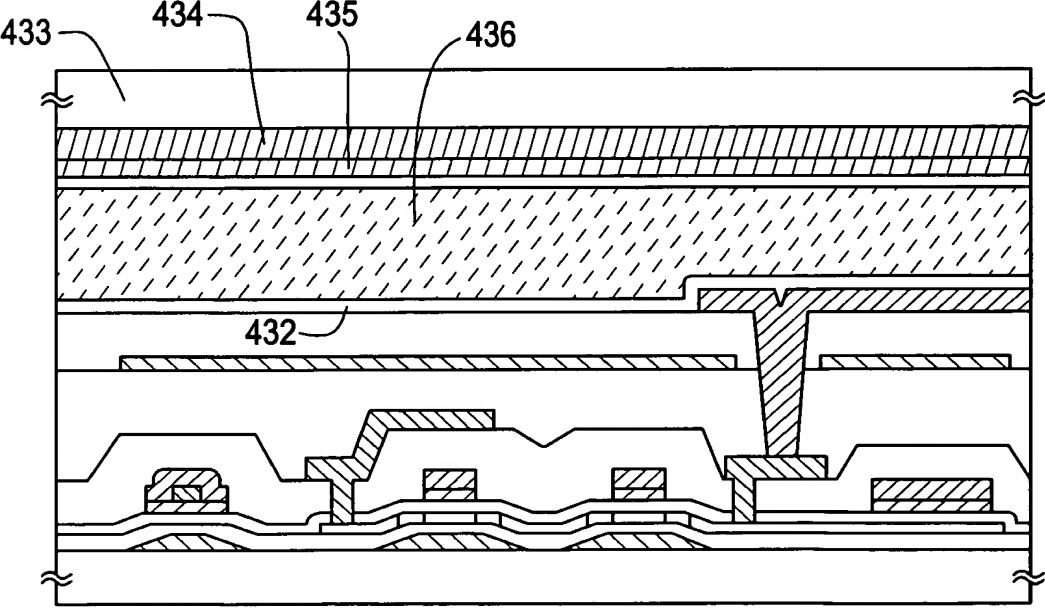


FIG. 6

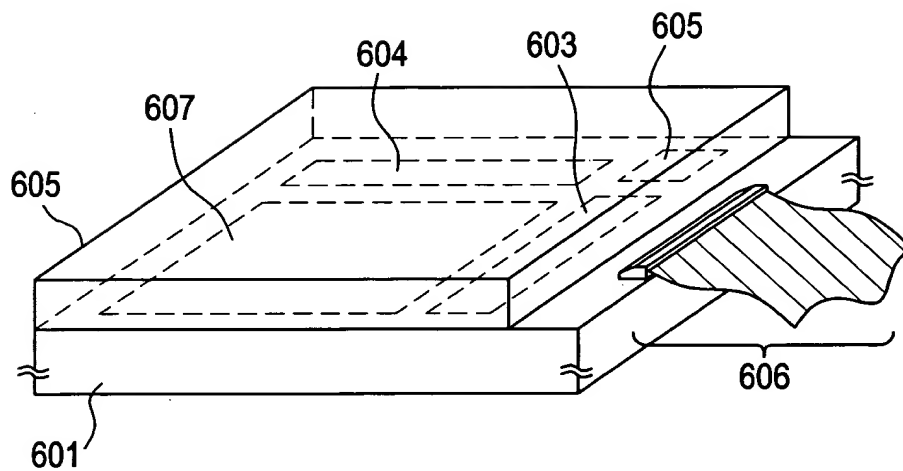


FIG. 7

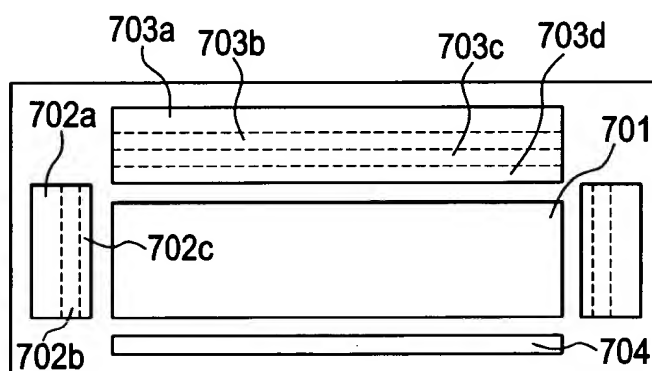


FIG. 8A

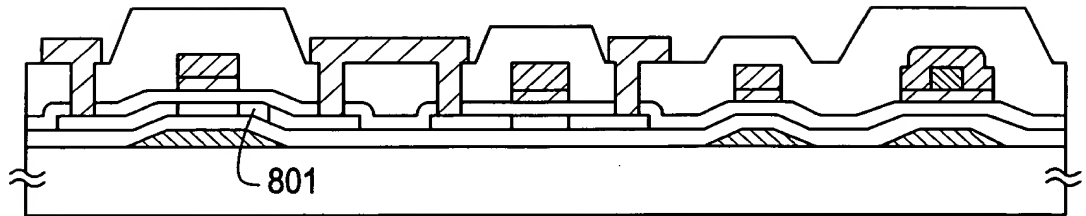


FIG. 8B

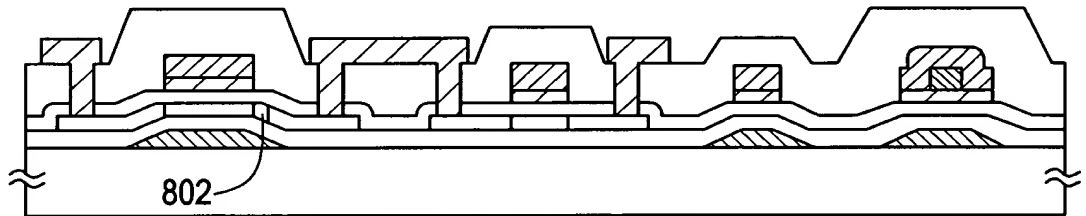


FIG. 8C

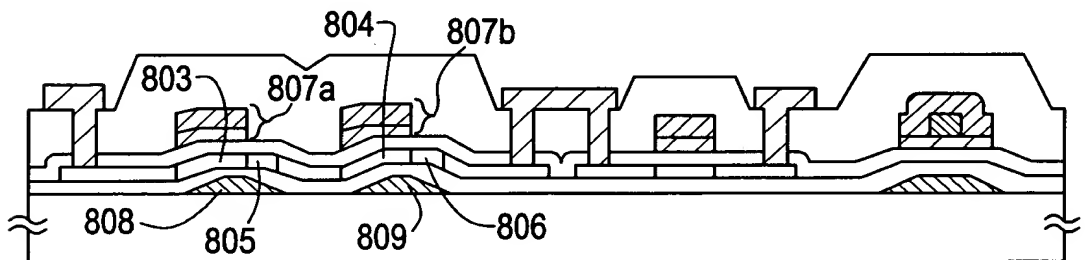


FIG. 8D

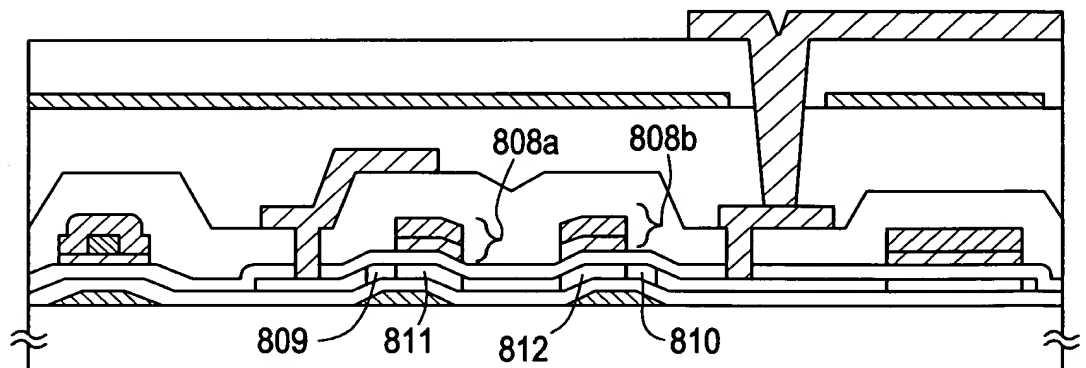
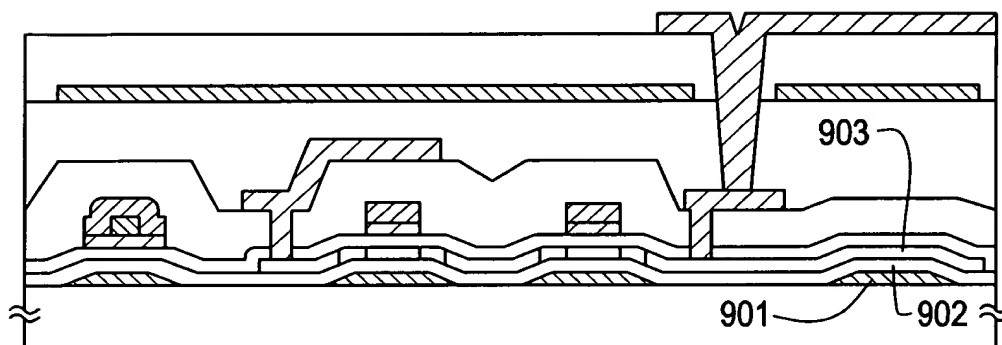


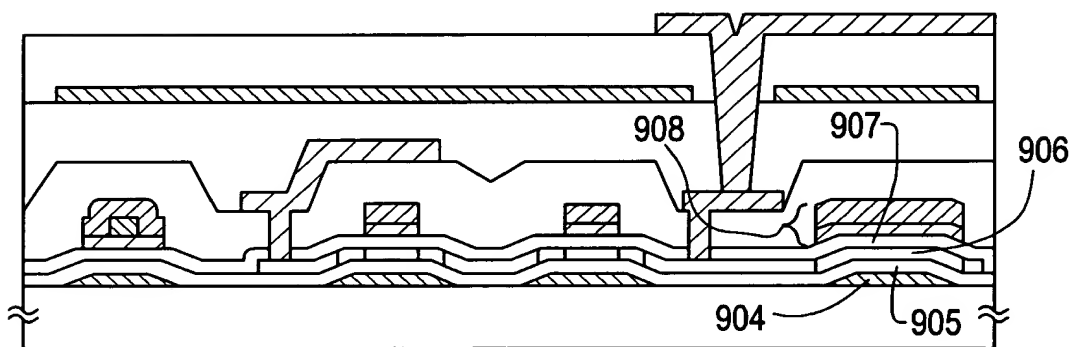
FIG. 9A



pixel TFT portion

storage capacitor portion

FIG. 9B



pixel TFT portion

storage capacitor portion

FIG. 9A

FIG. 10B

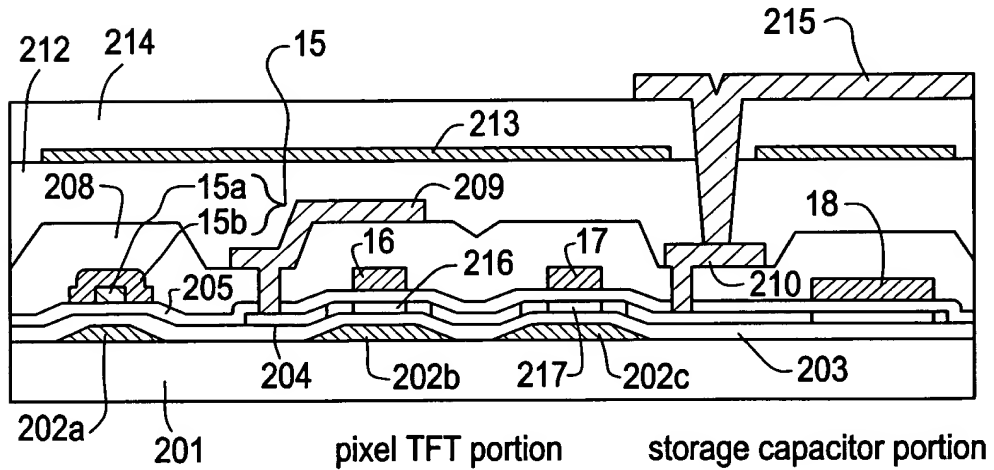


FIG. 11A

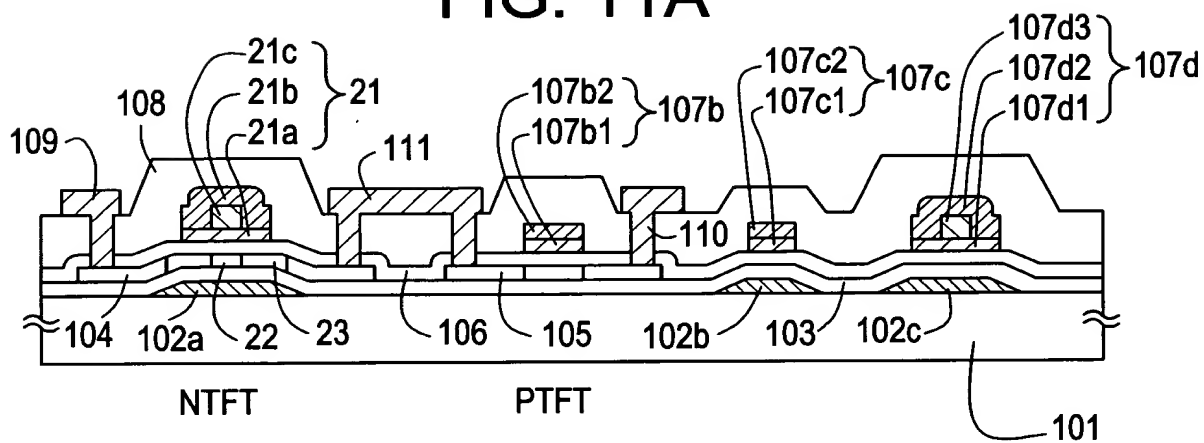


FIG. 11B

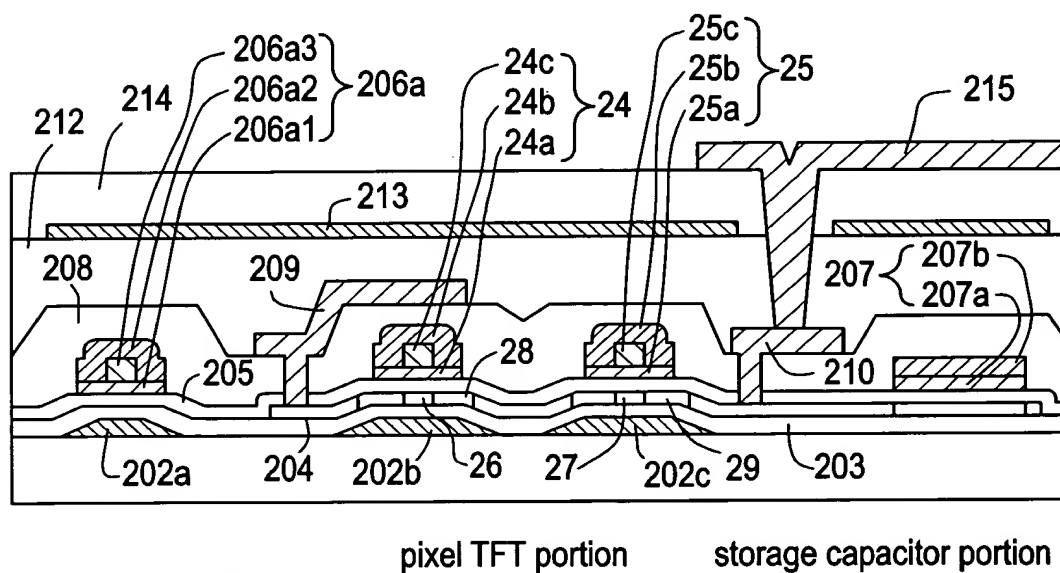
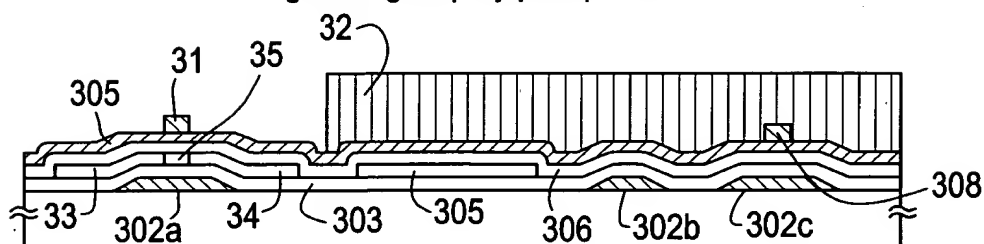
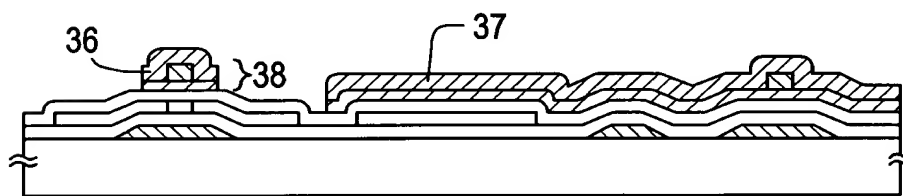
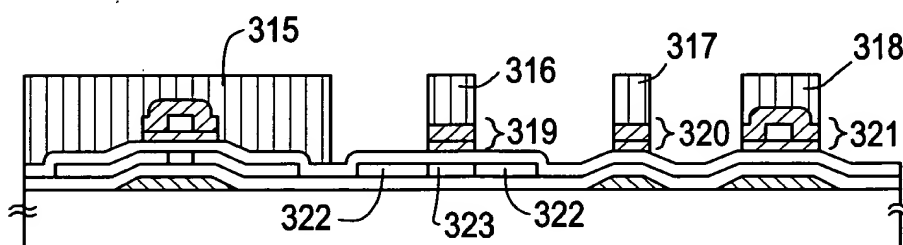


FIG. 12A

gettering step by phosphorus

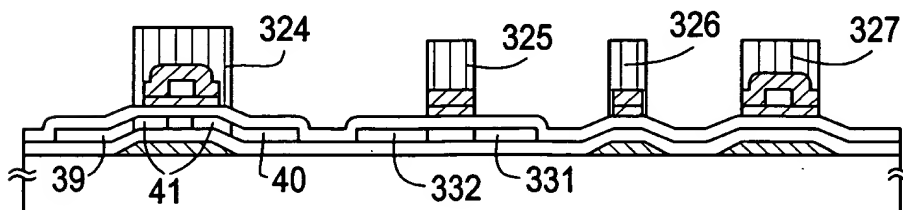
**FIG. 12B****FIG. 12C**

boron doping step

**FIG. 12D**

back side exposure step

phosphorus doping step



A detailed cross-sectional view of a pixel structure. The structure is divided into two main regions: NTFT (Non-Transparent Thin-Film Transistor) on the left and PTFT (Pixel Thin-Film Transistor) on the right. The base layer is labeled 101. Above it, there are several layers: 102a, 102b, 102c, 103, 104, 105, 106, 107a, 107b, 107c, 107d, 108, 109, 110, 111, 112, and 113. The PTFT region includes a gate stack (107a, 107b, 107c, 107d) and a channel layer (105). The NTFT region includes a gate stack (107a, 107b, 107c, 107d) and a channel layer (105). The structure is shown with various layers and components labeled with reference numerals.

A cross-sectional view of a semiconductor device. A substrate 328 is shown with a gate stack 330 on top. The gate stack 330 is composed of a gate dielectric 329 and a gate electrode 332. Source/drain regions 331 are formed on the substrate 328, adjacent to the gate stack 330. The source/drain regions 331 are doped with impurities, indicated by the hatching pattern. The gate electrode 332 is also doped with impurities, indicated by the hatching pattern. The gate dielectric 329 is formed on the gate electrode 332. The substrate 328 is formed on a base layer 327.

A cross-sectional diagram of a multi-layer printed circuit board (PCB). The diagram shows several layers: a top copper layer, a prepreg layer, and multiple internal layers of copper and prepreg. The layers are bonded together, and the diagram illustrates the internal structure of the board, including the copper cladding and the prepreg material.

FIG. 15A

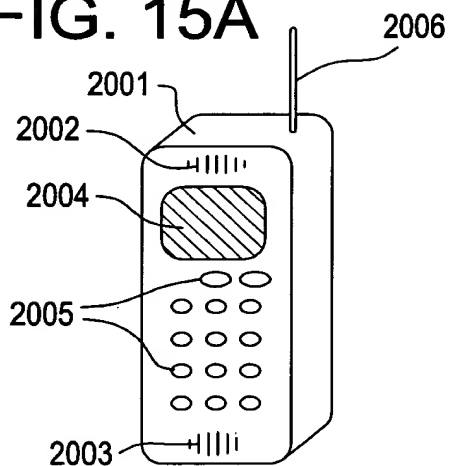


FIG. 15B

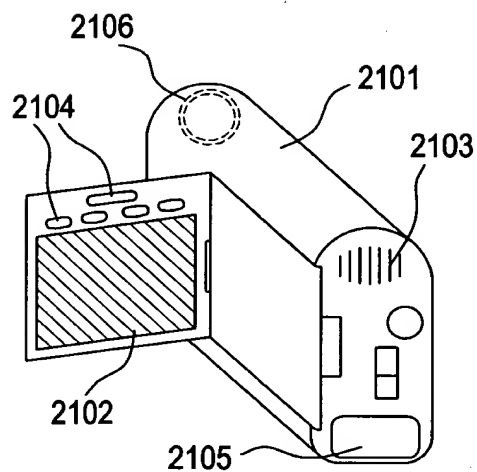


FIG. 15C

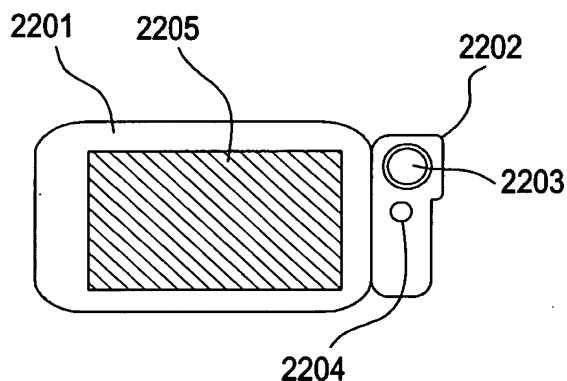


FIG. 15D

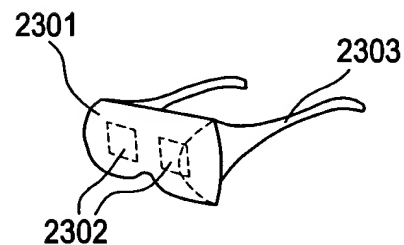


FIG. 15E

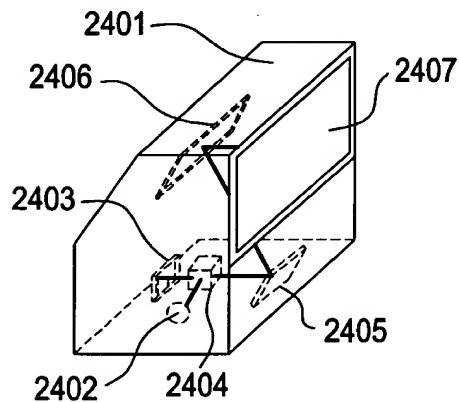


FIG. 15F

